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| EXAMINER | |
|---|---|
| CHAN, EMILY Y | |
| **ART UNIT** | **PAPER NUMBER** |
| 2829 | |

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,057 | THURAIRAJARATNAM ET AL. | |
| | Examiner | Art Unit | |
| | Emily Y Chan | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because no labels are provided for each element on Figs and 4. Bump pad 24 is recited on page 5 of specification but is shown in Figs 1-2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features that all probe pins of the probe card expect one pin are grounded recited in claim 12 and the probe card which is shorted with a disc and one in standing out recited in claim 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The disclosure is objected to because of the following informalities: "the reflected signal" and "the TDR signal" recited on page 5 of specification appears no antecedent basis.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. Claims 1-27 are s rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For example, the " interconnect impedance versus time data" recited in claims 1 and 15, all probe card pins except one pin grounded recited in claim 11 and "select the probe pin that is going to be the signal in the probe card and makes the rest of the pins ground" recited in claim 12 are critical or essential to the practice of the invention, but where the time data come from and how the interconnect impedance versus time data is generated are not explained in detail in the specification. Also when, and how to select the signal pin and make the rest of pins ground are not explained in detail in the specification. Furthermore, it is not explained where the post processing software is located and which device operates the software to obtain the interconnect impedance versus time in the specification.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1,11-15 and 23-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 15, it is unclear what the reflected signal stands for. The examiner assumes that the reflected signal is the measured interconnect impedance signal. The recitation that " provide interconnect impedance versus time data" is unclear

because it is not stated to where the interconnect impedance versus time data" is provided and where the time data come from originally.

In claim 10, it is not stated where the post processing software is. The examiner assumes it is in the tester since the tester which provide the interconnect impedance versus time data is recited in the claim 1.

In claims 11 and 24, the functions and structure that let probe card pins except one pin grounded are unclear since they are not fully explained in the specification.

In claims 12 and 25, how the tester head is configured to select the signal probe pin and makes the rest pins ground is unclear since they are not fully explained in the specification.

In claims 14 and 27, it is unknown where the "waveform" and the "data" come from. Also " the data" lacks antecedent basis.

***4. Provisional Rejections, 35 USC. 101, Double Patenting***

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims1-7, 9-11, 15-21 and 23-24 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-7, 10-12, 14-20 and 22-23 of copending

Application No. 10/448987. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

5. ***Provisional Rejection, Obviousness Type Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 8 and 22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9 and 21 of copending Application No. 10/448987. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two applications is that the claimed coaxial cable recited in claims 8 and 22 is connected to "the test head" and the coaxial cable recited in claims 9 and 21of copending Application No. 10/448987 is connected to "the probe card". Since the coaxial cable is used for transmitting signals only and the claimed probe card is mounted on the test head (see Fig. 1), it does not make patentable distinction from each other whether the coaxial cable is connected to the probe card or to the test head. This

is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Rutten ('726).

With respect to claims 1, 10 and 15, Hembree et al ('848) expressly teach a semiconductor probe card having resistance measuring circuitry (see Fig 3) and a method for measuring package interconnect impedance (resistivity contact) (see Col. 2, lines 53-56) as claimed, comprising:

a tester (26);

a device under test (DUT)/load board (10 and 12 and see Col. 4, lines 10-25) which is configured to retain a substrate (40 see Fig. 4 and Col. 6, line 44), and has signal wires which is connected to the tester (26), wherein the tester is configured to analyze a reflected signal and provide interconnect impedance versus time data (see Col. 8, lines 55-60);

A post processing software (see Fig 7), which is configured, to obtain interconnect impedance (resistance) versus time information.

Hembree et al ('848) do not teach a Digital Sampling Oseilloscope (DSO) which is configured to launch a signal received by the substrate (40) and to receive a reflected signal from the substrate (40) to the tester (26).

Rutten ('726) discloses a preconditioning integrated circuit (PCIC 350) in a test system (see Figs 3-5) and expressly teach a Digital Sampling Oseilloscope (DSO) (see Fig.5, OSC 530b) which is connected to a tester (310) and to a DUT (150) (see page 2, paragraph 0027). Moreover, Rutten ('726) teach that his Oseilloscope (DSO) is configured to launch a signal received by the DUT (150) (see Fig. 4) and to receive a reflected signal from the DUT (150) to the tester (310) (see page 2, paragraphs 0027-0028).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Rutten ('726) 's Digital Sampling Oscilloscope (DSO) into Hembree et al ('848)'s system so that a Digital Sampling Oscilloscope (DSO) is configured to connecte to the tester (26) and to the substrate (40) in Hembree et al ('848)'s system for the purpose of providing a test system for minimizing the adverse affects caused by long lead lines between a tester and a device under test as disclosed by Rutten ('726) (see page 1, paragraph 0009).

With respect to claims 2 and 16, Hembree et al ('848) teach a probe card (20) mounted to the tester (26) for contacting the substrate (40).

With respect to claims 3 and 17, Hembree et al ('848) teach that their tester (26) includes a tester head (30).

With respect to claims 4 and 18, Hembree et al ('848) teach that their probe card (20) is mounted to the tester head (26).

With respect to claims 5 and 19, Hembree et al ('848) teach that their probe card (20) has probe pins (22).

With respect to claims 6 and 20, Hembree et al ('848) teach that their probe pins (22) from the probe card (20) make contact with bump pads (44) on the substrate (see Col. 6, lines 17-23).

7. Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Rutten {'726) as applied to claim1, and further in view of Shahriari et al ('006).

Both Hembree et al ('848) and Magnuson ('790) do not disclose a socket, which is configured to hold the substrate for test.

Shahriari et al ('006) disclose a test socket system (see Fig 1a) and expressly teach a socket (106) wherein a package electronic circuit is mounted in a socket (106) for testing (see Col. 2, lines 47-48).

It would have been obvious to one of ordinary skilled in the art to incorporate the teaching of Shahriari et al ('006) 's socket (106) into Hembree et al ('848)'s and Rutten ('726)' s system so that a test socket is used to hold the substrate for test in order to provide more accuracy testing of electrical characteristics as disclosed by Shahriari et al ('006) (see Col.1 BACKGROUND).

8. Claims 8-9 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Rutten ('726) as applied to claims 1-2 and 15-16 respectively above, and further in view of Ayadi ('748).

With respect to claims 8 and 22, Hembree et al ('848) in view of Rutten ('726) do not teach a coaxial cable that connects the DSO to the test head.

With respect to claims 9 and 23, Hembree et al ('848) in view of Rutten ('726) do not teach a GPIB cable that connects the DSO to the tester.

Ayadi ('748) discloses a graphical user interface for testing integrated circuit (see Fig. 1) and expressly teach a coaxial cable (21) (see page 2, paragraph 0026, line 2) which connects the DSO (test instrument 13) to the probe card (20) and a GPIB cable (22) (see page 3, paragraph 0041, line 6-8) which connects the DSO (test instrument 13) to the tester (computer 23).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Ayadi ('748) 's coaxial and GPIB cables into Hembree et al ('848)'s and Rutten ('726)' s system so to ensure the communication between the test instruments and the tester or computer as disclosed by Ayadi ('748) (see page 3, paragraph 0042, lines 9-10).

9. Claims 11-14and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Rutten ('726) as applied to claims 1-2, 5 and 15-16 and 19 above, and further in view of Liu ('245).

With respect to claims 11-12 and 24-25, Hembree et al ('848) teach that his tester head (see Figs 3-4) is configured to select a probe pin (probe contacts 22) to be

signal in the probe card (see Col. 5, lines 48-50 " when testing all the edges of a round wafer with a probe card that includes rectangular or square pattern of probe contacts 22, some patterns of probe contacts 22 will not have an associated device under test").

With respect to claims 14 and 27, Rutten ('726) teaches a test head (Fig. 4, 410) is configured to obtain a waveform (pulse signal) (see page 2, paragraph 1127, line 6) and store " the data" in a file (computer memory 320).

With respect to claims 13 and 26, Rutten ('726) teaches a test head (Fig. 4, 410) is configured to let DSO (see Fig. 5, OSC 530b) signal out the probe contacts (470) and allow a reflection from the DUT (150) to get back to the DSO (see page 3, paragraph 0028).

Both Hembree et al ('848) and of Rutten ('726) do not teach that their Probe card is configured with all except one pin grounded and their tester head is configured to make the rest pins ground.

Liu ('245) discloses a probe card with ground shield structure (see Figs 7 and 8) and expressly teach to make a number of specific testing pins (302) of the probe card ground (See Col.6, lines 12-14).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Liu ('245)'s making probe pins ground into Hembree et al ('848)'s and Rutten ('726)' s system since making rest probe contacts ground will reduce or eliminate the ground noise coupling effect between the adjacent chips during test as disclosed by Liu ('245) (see Col. 6, lines 16-17).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsai ('694) discloses a method for testing probing pins and expressly teaches when a probe pin is charged to measure a resistance, the other probe pins are grounded (Col. 4, lines 40-43).

Magnuson ('790) teaches a coaxial cable which connects a digital sample oscilloscope to a circuit board under test.

Mayder et al ('453) teach a digital sample oscilloscope connected to a tester for testing integrated circuit (see Figs. 1-2).

Jain et al ('486) teach an oscilloscope sends signals to a tester and DUT for testing integrated circuit (see Fig. 5).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y Chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 7033081233. The fax phone number for the organization where this application or proceeding is assigned is 7038729306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

Ec
11-24-03

David A. Zarneke
Primary Exar
11/26/3